Abstract

Slave circuit having a data transmission interface (2) for processing data frames; an address register (10) for storing an address; a comparator (13) for comparing the address stored in the address register (10) with an address transmitted to the data transmission interface (2) in a data frame; an indicator register (16) which indicates the initialization of the slave circuit (1) if the address transmitted to the data transmission interface (2) in the slave circuit (1) is identical to a predetermined initialization address (UIA) for the slave circuit (1).

(Figure 6)

List of reference numerals

1	Slave circuit
2	Data transmission interface
3	Line
4	Data input
5	Clock input
6	Line
7	External data bus
8	Data processing unit
9	Internal address bus
10	Address register
11	Lines
12	Lines
13	Comparator
14	Lines
15	Indicator line
16	Indicator register
17	Indicator line
18	Control line
19	Inhibit logic unit
20	Input
21	Line
22	Input
23	Data output
24	Output
25	Line
26	Synchronization flipflop
27	Output
28	Line
29	Slave circuit output
30	Master circuit
31	Clock line
32	Data line
33	Data line
34	Data output
35	Data line

36 Data input

37 OR gate

38 AND gate